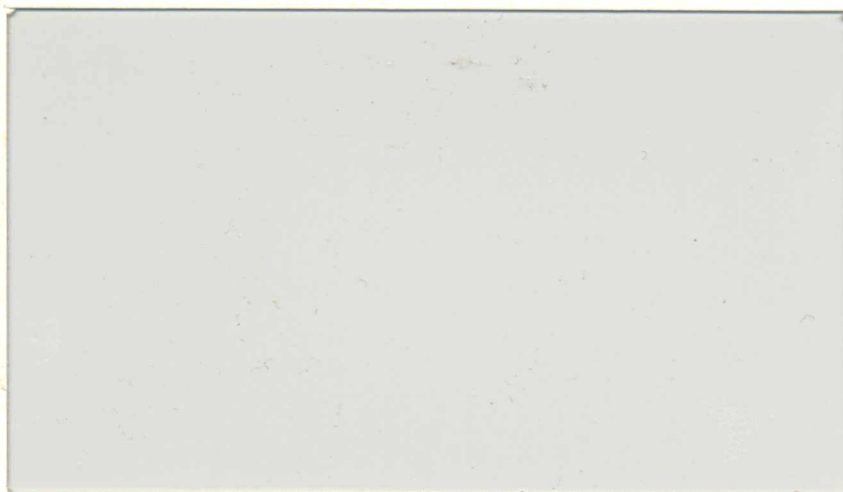




QBX÷FST

FAIL SAFE TIMER

QBX-FST

Product:÷ QBX-FST

Product Number:÷ 1006

Manual Number:÷ 1006÷01

Chapter	Rev	Note
All	1.0	1

Notes:÷

1.Original Document

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CHAPTER 1 GENERAL

Introduction

The QBX-FST is one of a growing range of SBX bus compatible boards manufactured by R & D Electronics. These boards are designed to increase the number of functions in a Multibus system without having to resort to a full Multibus card to achieve that function. This document provides all the information required to use the QBX-FST.

Description

The QBX-FST is a module that should be designed into every MULTIBUS system. It provides failsafe operation for the system plus several other features. The user is referred to two excellent Intel publications that discuss problems regarding random errors in the operation of microcomputers. They are "Designing Reliable Software for Automotive Applications" (AR102) and "Designing Microcontroller Systems for Electrically Noisy Environments" (AP-125). These two documents describe the likely cause of unpredictable faults that are not due to software problems. Two further articles, not directly related to the QBX-FST, but will give the user further insight in creating a more reliable product are:

Software Fault Tolerance Staves Off the Errors that Besiege Microprocessor Systems, Dick Jarret, Electronic Design, August 9 1984.

Fault Tolerant Software In Real Time Single Chip Microcontroller Systems, N.Q. Burnham and C.F. Cowling, Electronic Component and Applications (the Philips in house magazine), Vol 6, No 1, 1984.

Erratic computer behaviour can prove expensive. It requires time to debug, if indeed the problem is a result of circumstances interacting with software or hardware. It could just as easily be the result of environmental electrical noise. If this equipment is only erratic on site (and Murphy's Law dictates that the site is 1000 miles away) and the error only occurs every 9 days the costs are multiplied. The cost in customer relations may be even higher. The ability to automatically reset in the case of failure and to gracefully recover is essential in every system.

The QBX-FST caters for this need in MULTIBUS systems. It consists of two retriggerable monostable timers gated together, so that if either one should fail a reset pulse or an interrupt is issued to the system.

The QBX-FST may also be used in multimaster MULTIBUS systems when mounted on boards such as the R & D Electronics QBC-QBX (Quad SBX connector uncommitted MULTIBUS board) or the Intel iSBC 215 (Winchester controller with SBX connectors). Each master

could clock its own individual timer, or one could set and the other reset the clock.

In many projects the system must control several external devices such as solenoids, relays etc. Specified for a reaction time of several hundred milliseconds, the power up and intialisation is sometimes long enough to initiate an unwanted process. In addition the QBX-FST has an output that may be used to enable this external devices only when known conditions exist on the system I/O (e.g. such as on power up). It will also disable this hardware on system failure.

There is a facility for the detection of cold or warm starts to detect if in fact certain intialisation routines need be executed and visual indication of warm starts, resets and timeout failures.

Further there is an AC input to allow detection of AC failure, and finally there is a single buffered output bit for any user application.

Equipment Supplied

The QBX-FST is shipped in a padded package. Included in the packet are 2 plastic screws and a plastic spacer to mount the board on a host SBC type board.

Specifications

Access Time:

Write time: 45 nSec (max)

Read time: 45 nSec (max)

Addressing Range:

The QBX-FST is compatible with any board that supports the Intel SBX bus. The addressing range of the QBX-FST is derived from this host board.

QBX-FST outputs:

XEN and OUTA:

Output voltage: open collector Darlington

Maximum output voltage: 50 Volts DC

Output current sink: 200 mA on all outputs; outputs not TTL compatible.

XRST:

Output voltage: VMOS drain output with on board pull up resistor

Maximum output voltage: 60 Volts DC

Output current sink: 150mA; voltage proportional to this current

$r_{DS(on)}$: 7.5 ohms max

For further specs see data sheet on Motorola MC1413 or Sprague ULN 2003A and Siliconix VN2222L.

QBX-FST input:

Input voltage: AC input 40VAC max (set by programmable resistors)

Input current: Set by programmable resistors

Interface:

System Bus Compatible with the SBX bus specifications. See Intel publication 142686-001.

Interface connectors:

5/10 way, 0.1 inch spacing, compatible with Robinson-Nugent IDE-10 or similar.

Power Requirements:

5 Volts +/-5% @ 170 mA (max)

Environment:

Operating Temperature 0-55 degrees Celsius, humidity to 90% non-condensing.

Size:

Width- 72.4 mm (2.85 in)

Length- 94.0 mm (3.70 in)

Height- 20.6 mm (0.81 in)

CHAPTER 2 PRINCIPLE OF OPERATION

Introduction

This chapter describes the hardware operation of the QBX+FST. The user is recommended to read the two publications mentioned in Chapter 1.

QBX Bus Interface

Detailed description of the SBX bus is given in the Intel publication 142686-001. Users are referred to this document for a clearer understanding of its operation. The QBX+FST uses the following signals: MD0-MD2, MA0, MA1, MA2 CS0/, CS1/, IOWRT/, IORD/, MINTR0, MINTR1, and of course +5V, gnd and MPST/.

Overview

The principle behind the failsafe timer is that of continuously clocking a retriggerable monostable multivibrator. This maintains the output in an unstable state so that should a clock pulse fail to materialise within the monostable period, the output reverts to a stable state. This reversion provides a pulse that would normally be used to reset the computer.

On reset the software of the computer should interrogate the QBX+FST for cold or warm start status. If cold, then the contents of the memory may be initialised, say; if not then the contents of the memory could be checked for error but should not be altered unnecessarily.

Operation

(i) Normal Operation

As was discussed in the Intel documents mentioned in Chapter 1, it is possible for the microcomputer to clock a failsafe timer under failure conditions. To add protection the QBX+FST has two failsafe timers gated together to provide the reset pulse, should either fail. As a further level of security the two timers cannot be clocked simultaneously as they are located at different addresses.

The outputs are driven from an 8 bit addressable latch (U5) which is a 74LS259. This device has only one data input, driven from D0. The bit to be written to is addresses by the address lines MA0 to MA2, so that only one bit can be accessed at a given time. Addressing a particular bit and writing to it will transfer the information on the data input to the addressed output. Whilst there are 8 bits only 4 are used.

Writing a byte with $D0=1$ to the location associated with $A0=A1=A2=CS0=0$ will clock the monostable U6A, generating MONA. Writing to the same location with $D0=0$ will clear this line and must be done prior to re-clocking the monostable.

In a similar manner writing the same data to the address $A1=A2=CS0$, and $A1=1$ will clock the second monostable (U8A) generating MONB. This too, must be reset before it can be clocked again.

Once both MONA and MONB are active (logical high) the output of the NAND gate U7/3 is at a logical low. If, at any stage, both MONA and MONB are not high simultaneously this output will go high and this positive going edge will clock the reset monostable U6B.

The QBX-FST may be set up as a single failsafe timer by opening link Le thus permanently enabling this input to U7.

(ii) Failure

When U6B is clocked the Q output goes high for a predetermined period. This period must be long enough to reset all the devices connected to the system reset (if the QBX-FST is used to generate a reset pulse). In the instance of an active low reset signal link Lb should be closed and link La open. Alternatively the failure may be used to generate an interrupt (preferably non-maskable) or provide an active high reset pulse. In this case link Lb should be closed and link La open.

In either case the pulse will turn on the FAIL LED (RED LED-LED1) indicating that a failure has occurred. Pressing the SEEN switch (SW1) clears both the FAIL and RESET LEDs. These indicators are present to provide the system designer/ commissioning engineer with information of certain occurrences.

Note that in order for the failsafe system to be armed both MONA and MONB must be active. Until such time, if a failure occurs, no reset will occur.

(iii) Warm Start / Cold Start

When power is applied to the system a power on signal is generated by the capacitor C9/RP1 network. The output of both S-R flip flops (inputs connected in parallel) is set. The outputs may be cleared by writing a byte with $D0=1$ to location $A0=A2=CS0=0$ and $A1=1$.

One of these flip flop outputs (U2/9) is fed to D1 on a 3 state buffer. On reading any location with $CS1=0$ bit D1=1 means that the reset that occurred is due to a cold start. The other flip flop output drives the COLD START LED (GREEN LED - LED3). When activated a cold start has occurred but has not been cleared by the microprocessor. In order to aid in development a "SET COLD START" switch (SW2) is provided. This sets the flip flops into a cold start condition so that the system does not have to be powered

off and on whilst under In Circuit Emulation conditions.

(iv) XEN

In many applications a MULTIBUS system is used to control external devices such as solenoids etc. Whilst the specifications of such devices detail activation pulses of several hundred milliseconds, experience shows that power on and initialisation is enough to start a process in motion. The QBX-FST can alleviate this problem.

The output at U7/3 (the same that is used to clock the XRST/monostable) on reset is high and does not change state until the system is "armed", that is both MONA and MONB are active. If the system software only generates these signals once all initialisation is completed then the XEN signal can enable these external devices. In Figure 2.1a XEN is used to turn on a Solid State Relay that controls on the supply to the solenoids. Figure 2.1b uses a transistor with similar effect. Either polarity of XEN is available. With Lc open and Ld closed XEN is active low. With Lc closed and Ld open XEN is active high.

In a similar manner when a failure occurs XEN goes inactive (until initialisation is successfully completed) and so the external world is disabled when the computer is "down".

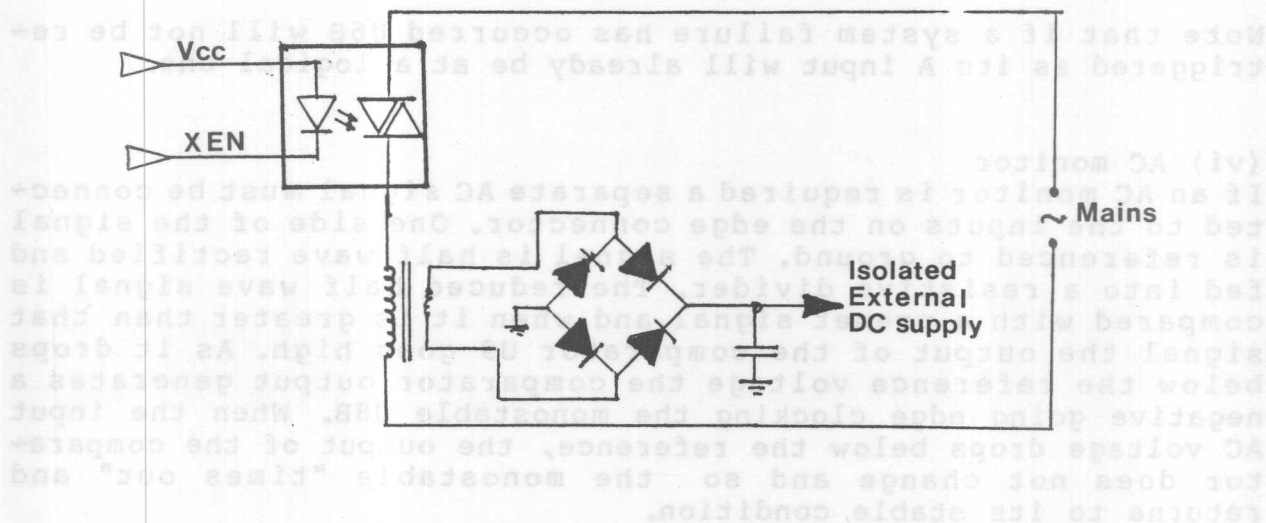


Figure 2.1a
Activation of Solid State Relay

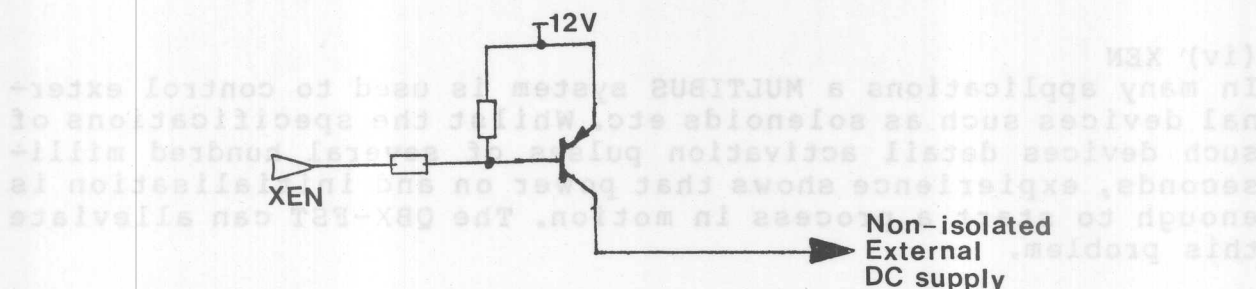


Figure 2.1b
Activation of Transistor

(v) Initialisation

On a system reset (irrespective of source) the QBX line RST goes active. This clears all the outputs of the 8 bit addressable latch (U5), holds monostables U6A, U8A and U8B in a clear condition on turns on the RESET LED (yellow LED+ LED2). The outputs of U6A and U8A are low (MONA and MONB respectively).

If the reset is due to a power up condition, the reset failure (XRST/) generator is held in the stable condition. If the reset is due to the panel reset being activated then U6B will be triggered. This will result in a sequence of events similar to that in system failure above. The only problem with this is that neither the system nor the engineer (via the LEDs) can distinguish this case from a timeout failure.

Note that if a system failure has occurred U6B will not be re-triggered as its A input will already be at a logical one.

(vi) AC monitor

If an AC monitor is required a separate AC signal must be connected to the inputs on the edge connector. One side of the signal is referenced to ground. The signal is half wave rectified and fed into a resistive divider. The reduced half wave signal is compared with a preset signal and when it is greater than that signal the output of the comparator U9 goes high. As it drops below the reference voltage the comparator output generates a negative going edge clocking the monostable U8B. When the input AC voltage drops below the reference, the output of the comparator does not change and so the monostable "times out" and returns to its stable condition.

This return can be used to generate an interrupt and its state may be interrogated by reading bit 2 at any address with CS1=0. The time before interrupt may be adjusted to allow for voltage fluctuations as may the reference voltage (set by RV). It must be borne in mind that the output of U9 will clock the monostable once in every mains cycle and so the period of the mains is the minimum monostable time period.

(vii) Single Bit Output

The output Q3 of the 8 bit addressable latch (U5) is fed into a spare input of the MC1413 and thus buffered by the Darlington transistor is brought out to the edge connector for uncommitted use.

CHAPTER 3 PROGRAMMING INFORMATION

Introduction

All the information required to programme the QBX-FST is contained in this chapter. This includes hardware and software configuration.

Monostables Pulse Length

There are four monostable flip flops contained in two packages (U6 and U8) on the QBX-FST. These flip flops are configured as retrigerrable, i.e. at each clock edge on the monostable input results in the start of a new monostable period, even if one is already in progress. The devices used are CMOS MC14538. The time period is determined by a resistive / capacitive network as shown in figure 3.1.

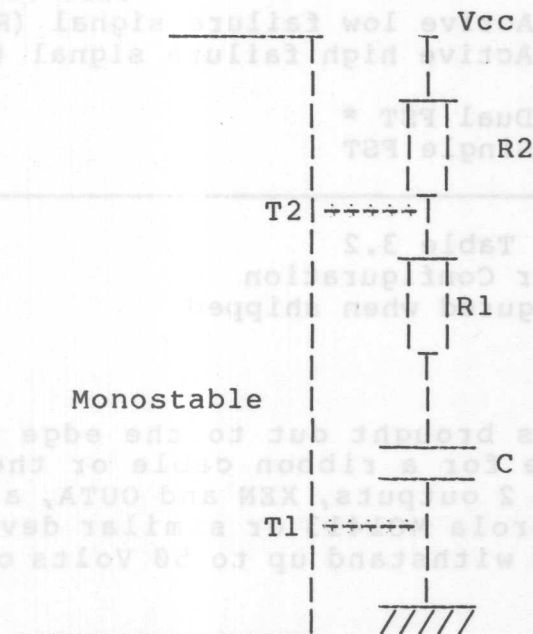


Figure 3.1
Monostable Timing Network

R1 is used to protect the 4538 against catastrophic failure in powering the system down. It is required to limit the discharge current to 10 mA when pin 16 (VDD) goes instantaneously to VSS. It is derived from the equation $R1 = ((VDD + 0.625) / (0.01)) + 250$. For VDD = 5V R1 is calculated to be nominally 220 ohms. The period of each monostable is given by the equation :-

$$T = (R1 + R2) * C$$

By varying the values of R2 and C different periods may be attained. The unit is shipped with values to give the nominal monostable periods listed in Table 3.1.

Monostable	Function	Period	C ÷ Value	R ÷ Value
U6A	MONA	47 mS	C11 ÷ 1uF	R8 ÷ 47 K
U8A	MONB	47 mS	C13 ÷ 1uF	R5 ÷ 47 K
U6B	XRST/	10 mS	C12 ÷ 1uF	R7 ÷ 10 K
U8A	ACLO/	27 mS	C8 ÷ 1uF	R3 ÷ 27 K

Table 3.1
Monostable Time Periods

Links

There are several options that can be implemented on the QBX-FST by configuring different links. Table 3.2 lists the different options.

Links	Result
Lc open, Ld closed	XEN active low *
Lc closed, Ld open	XEN active high (open collector)
La open, Lb closed	Active low failure signal (RESET) *
La closed, Lb open	Active high failure signal (INT0)
Le closed	Dual FST *
Le open	Single FST

Table 3.2
Jumper Configuration
* Configured when shipped

Outputs

There are 3 output signals brought out to the edge connector. This connector is suitable for a ribbon cable or the supplied connector may be used. The 2 outputs, XEN and OUTA, are derived from the outputs of a Motorola MC1413 or similar device. These output can sink 200 mA and withstand up to 50 Volts on the open collector output.

The last output signal is XRST which may be configured active high or active low. Besides being brought out on the edge connector it is also brought out on the INT0 line of the SBX connector. The reset signal may be connected externally to the signals INIT/ (pin 14 on P1) or AUX RESET/ (pin 38 on P2, if implemented). To save the external connection the usual wire wrap pin on the host board associated with INT0 may be connected by jumpers to these points. Alternatively the signal may be used to generate an interrupt. Since in failure a particular interrupt may be disabled this interrupt line should be non-maskable.

The output drive of this signal is via a VMOS transistor. In its on state r_{DS} is 7.5 ohms. Therefore the maximum current it can sink is 80 mA to guarantee a digital low signal. Note that the pull up resistor R16 is a low value and may in fact be in

parallel with a high value resistor in the reset circuitry. This would obviously interfere with the correct reset operation, so R16 should be removed.

Interrupt

Both interrupts MINT0 and MINT1 are used on the QBX-FST. They are not jumper configurable and it is up to the user to set them up on the host board if they are required. MINT0 can be used for failure detection, and MINT1 is used for AC LOW interrupts. Note the resistance values required as mentioned above.

Edge Conn. Pin	Function
1	GND
2	GND
3	XEN
4	
5	OUTA
6	XRST
7	Vcc
8	
9	AC IN
10	GND(AC IN)

Table 3.3
Pinout Edge Connector

Input

There is only one input to the QBX-FST via the edge connector. This is the AC signal. It is assumed to be 5 VAC with the resistors set for 2.5 VAC RMS. The potentiometer RV may be adjusted to give the desired cutoff point. If the input voltage is changed are any other variation is required the values of R14 and R15 may be adjusted according to the following formula where Vc is the voltage fed into the comparator and Vin is the AC voltage present at the input

$$V_c = V_{in} (R_{15}) / (R_{14} + R_{15})$$

Address Allocation

Table 3.4 list the different address allocations of the QBX-FST and the different actions. In this table PQRS are bit values (P is most significant) determined by the addressing of the host board. Their value must be determined from the manual of this host board. @= Active.

Address	WR/	RD/	D0	D1	D2	D3-D7	Action
PQRS0000	@	1	1	X	X	X	Clock Mon. A
PQRS0000	@	1	0	X	X	X	Clear Clock Mon. A
PQRS0001	@	1	1	X	X	X	Clock Mon. B
PQRS0001	@	1	0	X	X	X	Clear Clock Mon. B
PQRS0010	@	1	1	X	X	X	Set Warm Start
PQRS0010	@	1	0	X	X	X	Reset Warm Start Ck
PQRS0011	@	1	1	X	X	X	Set OUTA
PQRS0011	@	1	0	X	X	X	Clear OUTA
PQRS1XXX	1	@	X	0	X	X	Warm Start
PQRS1XXX	1	@	X	1	X	X	Cold Start
PQRS1XXX	1	@	X	X	0	X	AC present
PQRS1XXX	1	@	X	X	1	X	AC failure

Table 3.4
QBX-FST Address Allocation

Activating the Monostables

In order to clock the monostable A a byte with D0=1 must be written to location PQRS0000 (binary). PQRS is determined by the host board. Before the monostable can be clocked again this line must be reset. To achieve this, a byte with D0=0 must be written to the above address, i.e. PQRS0000 binary.

Clocking of monostable B is similar except that all actions are at location PQRS0001 binary.

Using Cold Start / Warm Start

When power is switched on or SW2 is closed a flip flop is set to indicate a cold start. The computer can interrogate this status after reset to determine whether data in memory is valid (after a failure) or whether to clear (on initialisation). This status is available on D1 at location PQRS1XXX binary. (X is don't care). If bit 1 is a logical high then cold start conditions exist. If low then warm start conditions exist.

In order to convert from a cold start to a warm start the micro-computer, once it has seen the cold start, must clock the flip flop. To do this a byte with D0=1 must be written to location PQRS0010 binary. This generates a monostable pulse through an RC network which will toggle the R+S flip flop. It is good practice to reset this line although not entirely necessary. To achieve this a byte with D0=0 must be written to location PQRS0010 binary.

OUTA

In order to activate the output OUTA at the edge connector (active low) a byte with D0=1 must be written to location PQRS0011 binary. To de-activate this output (open collector) a byte with D0=0 must be written to the same address.

Application Hints

In order to make the application of the QBX+FST more "bullet-proof" some suggestions follow:

1. Some boards (such as the QBC+QBX) allow the I/O space to be Memory mapped or I/O mapped. The QBX+FST should be I/O mapped. Only an I/O instruction can then actually send an output to the monostables.
2. Clocking monostable A and B should be done from different routines, and resetting of the lines from still other routines. If by chance the system accidentally gets to a routine that clocks the monostable, hopefully it will not get to clock the other as well. If it does, it still has to get to the routines that will reset the clock lines, in order to provide a new edge for the monostable.
3. If the CPU board has a timeout for off board accesses then this timeout should be disabled. The rationale is that in any illegal accesses will freeze the processor until the QBX+FST has time to act.
4. In a multi-master environment, where the QBX+FST is mounted on a separate board such as the QBC+QBX up to 4 masters may be used. Each processor either clocks or resets the clock line to either monostable.

LED Description

Interpretation of the LEDs can be based on Table 3.5.

COLD START (Green)	RESET (Yellow)	FAIL (Red)	Interpretation
X	On	Off	Power on reset
	On	On	Timeout failure or reset button pressed
On	X	X	Power on reset not cleared or Cold Start Switch pressed
Off	X	X	Warm start setup by computer

Table 3.5
LED Interpretation
(X=don't care)

CHAPTER 4 PREPARATION FOR USE

Introduction

This chapter provides information on the installation of the QBX+FST on a host SBC board.

Unpacking

The QBX+TMR is shipped in a padded packet together with 1 plastic spacer and 2 plastic screws. On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local R & D Electronics representative. If you do open the package, please retain the packaging.

Configuration

Configure the jumper connections as required. This may be attained by fitting jumpers or by using wire+wrap connections.

Mounting

The QBX+TMR will mount on any SBC computer that allows an iSBX board. Affix the spacer with one of the screws to the host board. Mount the spacer in the hole corresponding to the only mounting hole on the QBX board. The QBX+TMR should now be mounted on the mating connector and affixed to the host board with the remaining screw.

When a QBX card is mounted on a host card, the resulting structure occupies an additional card slot above the SBC card. Bear this in mind when you allocate slots in a cardframe.

Edge Connector

Mate the edge connector to the QBX board if required. The connector (if needed) can be hand soldered or of the ribbon cable variety. Electro+Phoenix and Klippon make ribbon cable to screw terminal adaptors.

XRST may be configured active high or active low. Besides being brought out on the edge connector it is also brought out on the INT0 line of the SBX connector. The reset signal may be connected externally to the signals INIT/ (pin 14 on P1) or AUX RESET/ (pin 38 on P2, if implemented). To save the external connection the usual wire wrap pin on the host board associated with INT0 may be connected by jumpers to these points. Alternatively the signal may be used to generate an interrupt and connected to a suitable jumper on the host board. Note that the pull up resistor R16 is a low value and may in fact be in parallel with a high value resistor in the reset circuitry. This would obviously interfere with the correct reset operation, so R16 should be removed.

CHAPTER 5 SERVICE

Introduction

This chapter provides a parts list and a schematic diagram of the QBX-FST.

Parts List

Semiconductors:

U1	7 Darlington transistor buffer	MC1413
U2	quad NAND R+S flip flop	MC14044
U3	quad bus transceiver	74LS243
U4	quad 2 input NOR gate	74LS02
U5	8 bit addressable latch	74LS259
U6,8	dual CMOS precision monostable	MC14538
U7	quad CMOS NAND gate	MC14011
D1÷4	general purpose diodes	1N4001
LED1	Stanley triangular red	SPR 5532 TRI
LED2	Stanley triangular yellow	SPG 5532 TRI
LED1	Stanley triangular green	SPY 5532 TRI
T1	VMOS transistor	VN2222L

Capacitors:

C2,3,4,5,	ceramic	0.01uF
7		
C6,8,9,	tantalum 10V	1uF
10,11,12,13		

Resistors:

RP1	SIL resistor array Epitek 10K	L109÷103÷G
R1	1/4W 5%	4.7 Kohm
R2,7,14,15	1/4W 5%	10 Kohm
R3	1/4W 5%	27 Kohm
R4,6,9,13	1/4W 5%	220 ohm
R5,8	1/4W 5%	47 Kohm
R10,11,12	1/4W 5%	330 ohm
R16	1/4W 5%	1 Kohm
RV1	single turn pot	10K

Connector:

Viking 36 way SBX	LMP01KH18A01
10 Way Amphenol	

Switches:	C&K miniature pushbutton	TP11
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